REMARKS/ARGUMENTS

Claims 1-6 are currently pending in this application. Claims 1-3, 5 and 6 have been amended. In view of the above amendments and following remarks, applicant respectfully submits that the application is in condition for allowance. Applicant therefore, respectfully requests reconsideration and allowance of the application.

In the final rejection dated April 1, 2003 the Examiner rejected claims 1-6 under 35 U.S.C. 112 second paragraph as being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, the Examiner alleges that there is no support for "coupling the pad voltage to a bias." Applicant respectfully traverses this rejection.

Claim 1 recites "coupling the pad voltage to a bias_mid node to provide the bias voltage for the integrated circuit when the power supply is below the predetermined value." Applicant respectfully submits that Figure 12A of the present application and the corresponding text in the specification clearly teach that when the power supply voltage "V_{DDO} is low, the string of devices 1217 turns on and the pad voltage is coupled to Bias_Mid" (page 15, lines 34-35). Applicant therefore respectfully submits that claim 1 is fully supported by the specification and respectfully requests that the section 112 rejection of claim 1, and claims 2-4 that depend from claim 1 be withdrawn.

Similarly, the Examiner alleges that there is no support in the specification for "providing bias_mid" to the input of a first semiconductor device as recited in claim 5. Applicant respectfully traverses this rejection.

Claim 5 recites "providing bias_mid to an input electrode of the first semiconductor device such that the first semiconductor device will turn off when V_{DDO} - bias_mid is less than the threshold of the

first semiconductor device". Applicant respectfully submits that transistor 1213 of Figure 12A provides explicit support for the recited element. Applicant therefore respectfully requests that the 112 rejection of claim 5 be withdrawn.

The Examiner also alleges that claim 6 is indefinite because it contradicts elements recited in claim 5. Applicant respectfully traverses this rejection.

Claim 6 recites "wherein actuating a switch in response to the turn off of the first semiconductor device to couple Vpad to bias_mid comprises ... providing a turn on voltage for a fourth semiconductor device; and using the turn on of the fourth semiconductor device to couple Vpad to bias_mid." Applicant therefore respectfully submits that claim 6 properly limits an element recited in claim 5 and respectfully requests that the section 112 rejection of claim 6 be withdrawn.

The Examiner rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by Takiba et al. (U.S. Patent 5,208,488). Applicant respectfully traverses this rejection.

Independent claim 1 recites a method of protecting an integrated circuit from an over voltage comprised in part by "coupling a bias voltage for the integrated circuit to a gate of a PMOS (P-channel Metal Oxide Semiconductor) device when the power supply is below the predetermined value; and coupling the pad voltage to a bias_mid node to provide the bias voltage for the integrated circuit when the power supply is below the predetermined value." Applicant respectfully submits that Takiba et al. does not disclose or suggest the recited elements.

Rather, in the potential detection circuit of Takiba the "gates of PMOS transistor P5 and the NMOS transistor N11 are connected to the potential VDD." (Takiba et al., col. 4, lines 1-2). Thus in the potential detection circuit of Takiba et al. the gate of the first

semiconductor device is coupled to the power supply voltage and not to a bias_mid node as recited in claim 1 of the present invention. (underlining added for emphasis only).

Accordingly, applicant respectfully submits that claim 1 recites a novel and unobvious method over Takiba et al. and is therefore allowable. Applicant further submits that claims 2-4 that depend directly or indirectly on claim 1 are allowable as is claim 1 and for additional limitations recited therein.

Independent claim 5 recites a method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present comprised in part by "providing bias_mid to an input electrode of the first semiconductor device such that the first semiconductor device will turn off when VDDO - bias_mid is less than the threshold of the first semiconductor device." Applicant respectfully submits that Takiba et al. does not disclose or suggest the recited element.

The Examiner alleges that N11 of Takiba et al. reads on the first semiconductor device of claim 5. Applicant respectfully submits that the source of the NMOS transistor N11 of Takiba et al. is grounded and is not coupled to a bias voltage (bias_mid) as recited in claim 5. (Takiba et al., FIG. 2, col. 4, lines 1-3, underlining added for emphasis only). In addition, turning off N11 does not actuate a switch to couple a pad voltage to bias_mid as recited in claim 5. Accordingly, applicant respectfully submits that claim 5 recites a novel and unobvious method over Takiba and is therefore allowable. Applicant further submits that claim 6 that depends directly or indirectly on claim 5 is allowable as is claim 5 and for additional limitations recited therein.

It is therefore respectfully submitted that pending claims 1-6 are in condition for allowance, and an early notice of allowance is respectfully requested.

Respectfully submitted,

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